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CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A resistance variable memory element comprising:

a structure comprising at least one chalcogenide glass layer formed between a pair of electrodes, said layer being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in a second voltage range.

2. The memory element of claim 1 wherein said at least one chalcogenide glass layer comprises a plurality of chalcogenide glass layers.

3. The memory element of claim 1 further comprising at least two chalcogenide glass layers arranged to sandwich at least one metal-containing layer between said two chalcogenide glass layers.

4. The memory element of claim 1 wherein said at least one chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x},

wherein x = 18 to 43.

5. The memory element of claim 1 wherein said at least one chalcogenide glass layer stoichiometry is about $Ge_{40}Se_{60}$.

6. The memory element of claim 1 wherein said at least one chalcogenide glass layer has a thickness between about 100 Å and about 1000 Å.

7. The memory element of claim 1 wherein said at least one chalcogenide glass layer has a thickness of about 150 Å.

8. The memory element of claim 1, further comprising at least one metal containing layer disposed with said chalcogenide glass layer between said electrodes.

9. The memory element of claim 8 wherein said at least one metal containing layer comprises a silver-chalcogenide.

10. The memory element of claim 8 wherein said at least one metal containing layer comprises silver-selenide.

11. The memory element of claim 8 wherein said at least one metal containing layer comprises silver-sulfide.

12. The memory element of claim 8 wherein said at least one metal containing layer comprises silver-oxide.

13. The memory element of claim 8 wherein said at least one metal containing layer comprises silver-telluride.

14. The memory element of claim 8 wherein said at least one metal containing layer has a first thickness and said at least one chalcogenide glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

15. The memory element of claim 8 wherein said at least one metal containing layer has a first thickness and said at least one chalcogenide glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

16. The memory element of claim 8 wherein said at least one metal containing layer comprises a plurality of stacked metal containing layers.

17. The memory element of claim 16 where at least one of the stacked metal containing layers is a layer containing silver.

18. The memory element of claim 8 further comprising at least two metal containing layers and at least three chalcogenide glass layers arranged alternately.

19. The memory element of claim 1 wherein at least one of said at least one chalcogenide glass layers or said electrodes contains a metal dopant.

20. The memory element of claim 19 wherein said metal dopant comprises silver.

21. A resistance variable memory device comprising:

at least one memory element comprising at least one chalcogenide glass layer; and

a write circuit for applying a first positive voltage to said memory element to switch said memory element from a first resistance state to a second resistance state and for applying a second positive voltage to switch said memory element from said second resistance state to said first resistance state.

22. The memory device of claim 21 wherein said at least one silver-chalcogenide layer comprises silver-selenide.

23. The memory device of claim 21 wherein said at least one silver-chalcogenide layer comprises silver-sulfide.

24. The memory device of claim 21 wherein said at least one silver-chalcogenide layer comprises silver-oxide.

25. The memory device of claim 21 wherein said at least one silver-chalcogenide layer comprises silver-telluride.

26. The memory device of claim 21 wherein said chalcogenide glass material has the formula Ge_xSe_{100-x}, wherein x = 18 to 43.

27. The memory device of claim 26 wherein said chalcogenide glass material stoichiometry is about $Ge_{40}Se_{60}$.

28. The memory device of claim 21 wherein at least one of said chalcogenide glass layers or said electrodes contains a metal dopant.

29. The memory device of claim 28 wherein said metal dopant comprises silver.

30. The memory device of claim 21 comprising first and second silver-chalcogenide layers, wherein said first silver-chalcogenide layer has a first thickness, said second chalcogenide glass layer has a second thickness, and a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

31. The memory device of claim 30 wherein said silver-chalcogenide layer has a first thickness, said second chalcogenide glass layer has a second thickness, and a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

32. The memory element of claim 30, wherein at least one of said first and second chalcogenide glass layers contains a metal dopant.

33. The memory element of claim 32 wherein said metal dopant comprises silver.

34. A memory element comprising:

a first electrode;

a first glass layer comprising Ge_xSe_{100-x}, wherein x = 18 to 43, said first glass layer being electrically coupled with said first electrode;

a first metal containing layer in contact with said first glass layer;

a second chalcogenide glass layer in contact with said first metal containing layer; and

a second electrode electrically coupled with said second chalcogenide glass layer, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in an second voltage range.

35. The memory element of claim 34 wherein x is about 40.

36. The memory element of claim 34 wherein said first metal containing layer comprises a silver-chalcogenide.

37. The memory element of claim 34 wherein said first metal containing layer comprises silver-selenide.

38. The memory element of claim 34 wherein said first metal containing layer comprises silver-sulfide.

39. The memory element of claim 34 wherein said first metal containing layer comprises silver-oxide.

40. The memory element of claim 34 wherein said first metal containing layer comprises silver-telluride.

41. The memory element of claim 34 wherein said first metal containing layer comprises a plurality of metal containing layers in serial contact with each other.

42. The memory element of claim 34 wherein at least one of said first glass layer and said second chalcogenide glass layer comprises a plurality of glass layers in serial contact with each other.

43. The memory element of claim 34 wherein at least one of said first and second chalcogenide glass layers contains a metal dopant.

44. The memory element of claim 43 wherein said metal dopant comprises silver.

45. A chalcogenide glass stack comprising:

a chalcogenide glass layer;

at least one metal containing layer in contact with said chalcogenide glass layer; and

a second chalcogenide glass layer in contact with said metal containing layer, said chalcogenide glass stack being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in an second voltage range different from said first voltage range.

46. The chalcogenide glass stack of claim 45 further comprising a metal containing electrode in electrical communication with said second chalcogenide glass layer .

47. The chalcogenide glass stack of claim 45 wherein said at least one metal containing layer comprises a silver-chalcogenide.

48. The chalcogenide glass stack of claim 45 wherein said at least one metal containing layer comprises silver-selenide.

49. The chalcogenide glass stack of claim 45 wherein said at least one metal containing layer comprises silver-sulfide.

50. The chalcogenide glass stack of claim 45 wherein said at least one metal containing layer comprises silver-oxide.

51. The chalcogenide glass stack of claim 45 wherein said at least one metal containing layer comprises silver-telluride.

52. The chalcogenide glass stack of claim 45 wherein at least one or both of said chalcogenide glass layers contains a metal dopant.

53. The chalcogenide glass stack of claim 52 wherein said metal dopant comprises silver.

54. A memory element comprising:

a first electrode;

at least one first chalcogenide glass layer in electrical communication with said first electrode;

at least one first metal containing layer in contact with said at least one first chalcogenide glass layer;

at least one second chalcogenide glass layer in contact with said at least one first metal containing layer;

at least one second metal containing layer in contact with said at least one second chalcogenide glass layer;

at least one third chalcogenide glass layer in contact with said at least one second metal containing layer; and

a second electrode in electrical communication with said at least one third chalcogenide glass layer, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in an second voltage range, said second voltage range being different from the first voltage range.

55. The memory element of claim 54 wherein said metal containing layers comprise one or more silver-selenide layers.

56. The memory element of claim 54 wherein one or more of said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

57. The memory element of claim 54 wherein one or more of said metal containing layers comprises a plurality of metal containing layers.

58. The memory element of claim 54 wherein one or more of said chalcogenide glass layers contains a metal dopant.

59. The memory element of claim 58 wherein said metal dopant comprises silver.

60. A method of forming a resistance variable memory element comprising the steps of:

forming a first electrode;

forming a first chalcogenide glass layer in contact with said first electrode;

forming a first metal containing layer in contact with said first chalcogenide glass layer; and

forming a second chalcogenide glass layer in electrical communication with said first metal containing layer;

forming a second metal containing layer in contact with said first chalcogenide glass layer;

forming a third chalcogenide glass layer in contact with said second metal containing layer; and

forming a second electrode in electrical communication with said third chalcogenide glass layer, said memory element being constructed and arranged

such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in an second voltage range.

61. The method of claim 60 wherein said chalcogenide glass layers comprise a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 43.

62. The method of claim 61 wherein said chalcogenide glass layers have a stoichiometry of about $Ge_{40}Se_{60}$.

63. The method of claim 60 wherein said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

64. The method of claim 60 wherein said metal containing layers comprise a plurality of metal containing layers.

65. The method of claim 60 wherein one or more of said chalcogenide glass layers contain a metal dopant.

66. The method of claim 60 wherein one or more of said metal containing layers comprises silver-selenide.

67. The method of claim 66 wherein said metal dopant comprises silver.

68. The method of claim 60 wherein said metal containing layers have a thickness which is equal to or greater than the thickness of each of said chalcogenide glass layers.

69. The method of claim 60 wherein each of said metal containing layers has a first thickness and each of said chalcogenide glass layers has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

70. The method of claim 69 further wherein said thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

71. A method of forming a resistance variable memory element comprising:

forming a first chalcogenide glass layer;

forming a silver-selenide layer in contact with said first glass layer; and

forming a second chalcogenide glass layer in contact with said silver-selenide layer, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a first positive voltage and from a lower to higher resistance state upon application of a positive voltage in an second voltage.

72. The method of claim 71 wherein said chalcogenide glass material has a stoichiometric composition of about $Ge_{40}Se_{60}$.

73. The method of claim 71 wherein at least one of said glass layers contains a metal dopant.

74. The method of claim 73 wherein said metal dopant comprises silver.

75. The method of claim 71 further comprising the step of forming alternating layers of said chalcogenide glass material and said silver-selenide layer.

76. The method of claim 71 wherein said layer formed of said chalcogenide glass material further contains a metal dopant.

77. The method of claim 76 wherein said metal dopant comprises silver.

78. The method of claim 71 wherein said metal containing layer has a thickness which is equal to or greater than a thickness of each of said first and second chalcogenide glass layers.

79. The method of claim 71 wherein said metal containing layer comprises a plurality of silver-selenide layers in serial contact with each other.

80. A processor-based system, comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit including a resistance variable memory element comprising at least one metal containing layer, at least one chalcogenide glass layer, at least one other chalcogenide glass layer, said metal containing layer being provided between said at least one chalcogenide glass layer and said at least one other chalcogenide glass layer, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a first positive voltage and from a lower to higher resistance state upon application of a second positive voltage.

81. The system of claim 80 wherein said chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x = 18 to 43.

82. The system of claim 81 wherein said chalcogenide glass layer stoichiometry is about $Ge_{40}Se_{60}$.

83. The system of claim 80 wherein at least one of said glass layers contains a metal dopant.

84. The system of claim 83 wherein said metal dopant comprises silver.

85. The system of claim 81 further comprising another metal containing layer in contact with said at least one other chalcogenide glass layer and at least one third chalcogenide glass layer in contact with said at least one second metal containing layer.

86. The system of claim 81 wherein said chalcogenide glass layers comprise a plurality of stacked chalcogenide glass layers.

87. The system of claim 81 wherein said metal containing layer comprises a plurality of stacked metal containing layers.

88. The system of claim 81 wherein at least one of said chalcogenide glass layers comprises a metal dopant.

89. The system of claim 81 wherein said metal containing layer comprises a silver-selenide layer.

90. A processor-based system, comprising:

a processor;

a memory circuit connected to said processor, said memory circuit comprising a first electrode;

at least one first chalcogenide glass layer in electrical communication with said first electrode;

at least one first metal containing layer in contact with said at least one first chalcogenide glass layer;

at least one second chalcogenide glass layer in contact with said at least one first metal containing layer;

at least one second metal containing layer in contact with said at least one second chalcogenide glass layer;

at least one third chalcogenide glass layer in contact with said at least one second metal containing layer; and

a second electrode in electrical communication with said at least one third chalcogenide glass layer, said memory circuit being constructed and arranged such that a resistance value of said memory circuit switches from a higher to lower resistance state upon application of a first positive voltage and from a lower to higher resistance state upon application of a second positive voltage.

91. The system of claim 90 wherein said metal containing layers comprise one or more silver-selenide layers.

92. The system of claim 91 wherein one or more of said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

93. The system of claim 90 wherein one or more of said metal containing layers comprises a plurality of metal containing layers.

94. The system of claim 90 wherein one or more of said chalcogenide glass layers contains a metal dopant.

95. The system of claim 94 wherein said metal dopant comprises silver.

96. A memory element comprising:

a first electrode;

a second electrode; and

a plurality of chalcogenide glass layers and at least one metal containing layers arranged between said first and second electrodes, whereby said plurality of chalcogenide glass layers alternate with said at least one metal containing layers, with one of said chalcogenide glass layers being in contact with said first electrode and another of said chalcogenide glass layers being in contact with said second electrode, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in an second voltage range.

97. The memory element of claim 96 wherein said at least one metal containing layers comprises one or more silver-selenide layers.

98. The memory element of claim 96 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

99. The memory element of claim 96 wherein one or more of said at least one metal containing layers comprises a plurality of metal containing layers.

100. The memory element of claim 96 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

101. The memory element of claim 100 wherein said metal dopant comprises silver.

102. A method of forming a resistance variable memory element comprising:

forming a first electrode;

forming a second electrode; and

forming a plurality of chalcogenide glass layers and at least one metal containing layer between said first and second electrodes, whereby said plurality of chalcogenide glass layers alternate with said at least one metal containing layers, with one of said chalcogenide glass layers being in contact with said first electrode and another of said chalcogenide glass layers being in contact with said second electrode, said layers being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of first a positive voltage and from a lower to higher resistance state upon application of a second positive voltage.

103. The method of claim 102 wherein said at least one metal containing layers comprises one or more silver-selenide layers.

104. The method of claim 102 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

105. The method of claim 102 wherein one or more of said at least one metal containing layers comprises a plurality of metal containing layers.

106. The method of claim 102 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

107. The method of claim 106 wherein said metal dopant comprises silver.

108. A resistance variable memory element comprising a PCRAM stack including amorphous semiconducting glass layers separated by a layer of silver-containing material, wherein the resistance variable memory element switches to a low resistance state upon application of a first positive write pulse, and switches to a high resistance state by application of a second positive write pulse.

109. A resistance variable memory element as in claim 108 wherein the amorphous semiconducting glass layers include chalcogenide glass.

110. A resistance variable memory element as in claim 108 wherein a time duration of the first and second positive write pulses is less than about 8 nanoseconds.

111. A resistance variable memory element as in claim 108, wherein the first positive write pulse has a magnitude of between about 700 mV and about 1 V.

112. A resistance variable memory element as in claim 108 wherein the first positive write pulse has a magnitude of about 700 mV.

113. A resistance variable memory element as in claim 108 wherein the low resistance state is about 10K Ohm.

114. A resistance variable memory element as in claim 108 wherein the second positive write pulse has a magnitude of at least about 1.5 V.

115. A resistance variable memory element as in claim 114 wherein the high resistance state is in the Megohm range.

116. A resistance variable memory element comprising a PCRAM stack including amorphous semiconducting glass layers separated by a layer of silver-containing material, wherein a resistance value of the resistance variable memory element is switchable between two discrete states, one lower and the other high, upon application of respective positive voltages.